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EXAMINER	
RIYAMI, ABDULLA A	

ART UNIT	PAPER NUMBER
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/808,771	CIOFFI, JOHN M.	
	Examiner	Art Unit	
	ABDULLAH RIYAMI	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/19/2008 has been entered.

Claim Rejections - 35 USC § 103

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-7, 10-17, 20-26, and 35-38 are rejected under 35 U.S.C. 103 as being unpatentable by Tsatsanis et al. (US 2006/0056522 A1) in view of Henderson et al. (6678375).

As per claim 1, Tsatsanis et al. discloses a DSL system comprising:

a multiple loop segment, comprising K bonded loops providing up to (2K-1) communication channels (see paragraphs 48-50 and see figure 2, block 208 and figure 3); and a controller coupled to the multiple loop segment and configured to provide control signals used to operate the multiple loop segment as a vectored system (see paragraph 20, 54, 70-81, and 140, figure 5 and figure 11, block 1104 and 1108) by vectoring upstream and downstream transmissions with the plurality of CPEs across multiple active channels of the segment from the end of the multiple loop segment opposite the CPEs (see paragraph 40 (user equipment and multiplexers) and 43, local area network contains plurality of CPEs and figure 1 and 2).

Tsatsanis also discloses the segment being coupled at one end to a plurality of different customer premises equipment (CPE) to provide different channels to different

CPE's (see paragraph 40 and 43, local area network contains plurality of CPEs) (Henderson et al. also discloses this in column 4, lines 41-51)

Tsatsanis et al. does not expressly disclose each loop comprising 2 wires, one of the 2K wires being selected as a reference wire, the remaining (2K-1) wires being referenced to the reference wire.

Henderson et al. discloses each loop comprising 2 wires, one of the 2K wires being selected as a reference wire, the remaining (2K-1) wires being referenced to the reference wire (see figures 4 an 5, and column 3, lines 55-67 and column 4, lines 1-51).

Henderson et al. and Tsatsanis et al. are analogous art because they are from the same field of endeavor of DSL transmission.

At the time of the invention it would have been obvious to one of ordinary skill in the art to use Henderson et al.'s reference wire (see figure 4 or 5) technique in Tsatsanis et al. multiline transmission technique (fig 2).

The motivation to combine would have been to have a significant increase in speed for data transmission and the total data rate for transmission over twisted pairs can approach three times the data rate of previous data rate, substantially reducing the time for data transmission. By designating a common wire to support a plurality of lines, then more lines transmit data to provide much desired higher data rates.

As per claim 2, Tsatsanis et al. discloses a DSL system wherein the controller comprises vectoring control means, the DSL system further comprising a customer vectoring unit (CVU) is coupled to a first end of the multiple loop segment and to the vectoring means (see figure 2, blocks 210-1 and 216-1, figure 11, blocks 1104 and

1108) and a pedestal VU (PVU) is coupled to a second end of the segment and to the vectoring means (see figure 2, blocks 204-1 and 214-1, figure 11, blocks 1104 and 1108) vectoring upstream and downstream transmissions across multiple active channels (see paragraph 40).

As per claims 3 and 4, Tsatsanis et al. discloses a DSL system wherein the PVU is in a pedestal or first pedestal (see figure 2, blocks 204-1 to 204-N) and further wherein the CVU is in a customer premises or second pedestal (see figure 2, blocks 210-1 to 210-N).

As per claim 5, Tsatsanis et al. discloses a DSL system wherein the PVU comprises a vector signal-processing module coupled to the controller (see figure 11, block 1104 and figure 2, block 214-1) and further wherein the CVU comprises a vector signal-processing module coupled to the controller (see figure 11, block 1104 and 1108 and figure 2 block 216-1).

As per claim 6, Tsatsanis et al. discloses a DSL system wherein at least one of the communication channels is operated using an expanded frequency spectrum (see paragraph 70, and figure 2, block 208).

As per claim 7, Tsatsanis et al. discloses a DSL system wherein the controller comprises means for controlling the frequency bandwidth used in transmitting data across the segment (see paragraphs 70-71).

As per claim 10, Tsatsanis et al. discloses a DSL system comprising a first impedance matching circuit coupled to a first end of the segment (see figure 12); (see

figure a second impedance matching circuit coupled to a second end of the segment (see figure 12).

As per claim 11, Tsatsanis et al. discloses a DSL system, wherein the DSL system is an ADSL system (see paragraph 48, line 5).

As per claim 12, Tsatsanis et al. discloses a DSL system, wherein the DSL system is a VDSL system (see paragraph 48, line 5).

As per claim 13, Tsatsanis et al. discloses a DSL system, wherein the loops are bonded using one of the following bonding protocols: TDIM bonding; Ethernet bonding; ATM bonding; or the G.bond protocol (see twisted pair, paragraph 49, line 5).

As per claim 14, Tsatsanis et al. discloses a DSL system comprising:
a multiple loop segment, comprising K bonded loops providing up to (2K-1) communication channels on (2K- 1) wires (see paragraphs 48-50 and see figure 2, block 208 and figure 3); Tsatsanis also discloses the segment being coupled at one end to a plurality of different customer premises equipment (CPE) to provide different channels to different CPE's (see paragraph 40 and 43, local area network contains plurality of CPEs) (Henderson et al. also discloses this in column 4, lines 41-51), a first vectoring unit coupled to a first end of the segment and comprising a first vector signal processing module (see figure 2, blocks 204-1 and 214-1, figure 11, blocks 1104 and 1108) the first vectoring unit being resident at one of a plurality of different CPEs (see paragraph 18, transmitter, receiver and figure 2); a second vectoring unit coupled to a second end of the segment and comprising a second vector signal processing module (see figure 2, blocks 210-1 and 216-1, figure 11, blocks 1104 and 1108) opposite the

plurality of CPEs (see paragraph 18, transmitter, receiver and figure 2); and wherein the first and second vectoring units provide vectored transmissions across the segment (see paragraph 20, 54, 70-81, and 140), the second vectoring unit vectoring upstream and downstream transmissions with the plurality, of CPEs across all active channels of the segment (see paragraph 40 and 43, local area network contains plurality of CPEs) (Henderson et al. also discloses this in column 4, lines 41-51).

Tsatsanis et al. does not expressly disclose each loop comprising 2 wires, one of the 2K wires being selected as a reference wire, the remaining (2K-1) wires being referenced to the reference wire.

Henderson et al. discloses each loop comprising 2 wires, one of the 2K wires being selected as a reference wire, the remaining (2K-1) wires being referenced to the reference wire (see figures 4 an 5, and column 3, lines 55-67 and column 4, lines 1-51).

Henderson et al. and Tsatsanis et al. are analogous art because they are from the same field of endeavor of DSL transmission.

At the time of the invention it would have been obvious to one of ordinary skill in the art to use Henderson et al.'s reference wire (see figure 4 or 5) technique in Tsatsanis et al. multiline transmission technique (fig 2).

The motivation to combine would have been to have a significant increase in speed for data transmission and the total data rate for transmission over twisted pairs can approach three times the data rate of previous data rate, substantially reducing the time for data transmission. By designating a common wire to support a plurality of lines, then more lines transmit data to provide much desired higher data rates.

As per claim 15, Tsatsanis et al. discloses a DSL system comprising a controller coupled to the first (see figure 2, blocks 204-1 and 214-1, figure 11, blocks 1104 and 1108) and second vectoring units (see figure 2, blocks 204-1 and 214-1, figure 11, blocks 1104 and 1108), wherein the controller comprises vectoring control means, wherein the vectoring control means assists in regulating transmissions across the multiple loop segment (see paragraph 20, 54, 70-81, and 140).

As per claim 16 and 17, Tsatsanis et al. discloses a DSL system wherein the first vectoring unit is in a first pedestal (see figure 2, blocks 204-1 to 204-N) and further wherein the second vectoring unit is in a second pedestal or customer premises (see figure 2, blocks 210-1 to 210-N).

As per claim 20, Tsatsanis et al. discloses a DSL system comprising a first impedance matching circuit coupled to a first end of the multiple loop segment (see figure 12); (see figure a second impedance matching circuit coupled to a second end of the multiple loop segment (see figure 12).

As per claim 21, Tsatsanis et al. discloses a DSL system comprising: a multiple loop segment, comprising K bonded loops providing up to (2K-1) communication channels on (2K-1) wires (see paragraphs 48-50 and see figure 2, block 208 and figure 3); Tsatsanis also discloses the segment being coupled at one end to a plurality of different customer premises equipment (CPE) to provide different channels to different CPE's (see paragraph 40 and 43, local area network contains plurality of CPEs) (Henderson et al. also discloses this in column 4, lines 41-51); a first impedance matching circuit coupled to a first end of the segment (see figure 12); a first vector

signal processing module coupled to the first impedance matching circuit resident at one of a plurality of different CPEs (see paragraph 18, transmitter, receiver and figure 2) (see figure 2, blocks 204-1 and 214-1, figure 11, blocks 1104 and 1108 and figure 12); a second impedance matching circuit coupled to a second end of the segment (see figure 12); a second vector signal processing module coupled to the second impedance matching circuit opposite the plurality of CPEs (see paragraph 18, transmitter, receiver and figure 2) (see figure 2, blocks 210-1 and 216-1, figure 11, blocks 1104 and 1108 and figure 12); and a controller coupled to the first and second vector signal processing modules (see paragraph 20, 54, 70-81, and 140, figure 5 and figure 11, block 1104 and 1108) comprising: means for collecting data regarding transmissions across the multiple loop segment (see paragraph 20, 54, 70-81, and 140); and means for controlling vectoring of transmissions across the segment (see paragraph 20, 54, 70-81, and 140); wherein the first and second vector signal processing modules process transmissions across the multiple loop segment (see paragraph 20, 54, 70-81, and 140) so that the second vectoring unit vectoring upstream and downstream transmissions with the plurality, of CPEs across all active channels of the segment (see paragraph 40 and 43, local area network contains plurality of CPEs) (Henderson et al. also discloses this in column 4, lines 41-51). (The additional features of claim 21 regarding the impedance matching circuits are normal design options).

Tsatsanis et al. does not expressly disclose each loop comprising 2 wires, one of the 2K wires being selected as a reference wire, the remaining (2K-1) wires being referenced to the reference wire.

Henderson et al. discloses each loop comprising 2 wires, one of the 2K wires being selected as a reference wire, the remaining (2K-1) wires being referenced to the reference wire (see figures 4 an 5, and column 3, lines 55-67 and column 4, lines 1-51).

Henderson et al. and Tsatsanis et al. are analogous art because they are from the same field of endeavor of DSL transmission.

At the time of the invention it would have been obvious to one of ordinary skill in the art to use Henderson et al.'s reference wire (see figure 4 or 5) technique in Tsatsanis et al. multiline transmission technique (fig 2).

The motivation to combine would have been to have a significant increase in speed for data transmission and the total data rate for transmission over twisted pairs can approach three times the data rate of previous data rate, substantially reducing the time for data transmission. By designating a common wire to support a plurality of lines, then more lines transmit data to provide much desired higher data rates.

As per claim 22, Tsatsanis et al. discloses a DSL system wherein the first and second vector signal processing modules provide two-sided vectoring of transmissions across the multiple loop segment (see figure 5).

As per claim 23, Tsatsanis et al. discloses a DSL system wherein the first and second vector signal processing modules provide one-sided vectoring of transmissions across the multiple loop segment (see figure 5).

As per claim 24, Tsatsanis et al. discloses a DSL system wherein the multiple loop segment couples customer premises equipment to a pedestal (see figure 2).

As per claim 25, Tsatsanis et al. discloses a DSL system wherein the multiple loop segment couples a first pedestal to a second pedestal (see figure 2).

As per claim 26, Tsatsanis et al. discloses a method of sending high speed DSL service, the method comprising: sending a first signal through a first communications channel to a first customer premises equipment (CPE) using a first wire of a first one of multiple bonded loops (see paragraphs 48-50 and see figure 2, block 208 and figure 3); sending a second signal through a second communications channel to a second CPE using a second wire of a second one of the multiple bonded loops of the multiple loop segment (see paragraphs 48-50 and see figure 2, block 208 and figure 3); and vectoring upstream and downstream transmissions (see paragraph 40 and 43, local area network contains plurality of CPEs) (Henderson et al. also discloses this in column 4, lines 41-51) through the communications channels across the multiple loop segment across both communications channels from an upstream location (see paragraph 20, 54, 70-81, and 140, figure 5 and figure 11, block 1104 and 1108).

Tsatsanis et al. does not expressly a reference wire of a multiple loop segment and the reference wire of the first channel and the common reference wire being a wire of a bonded loop of the multiple loop segment.

Henderson et al. discloses a reference wire of a multiple loop segment and the reference wire of the first channel and the common reference wire being a wire of a bonded loop of the multiple loop segment (see figures 4 an 5, and column 3, lines 55-67 and column 4, lines 1-51).

Henderson et al. and Tsatsanis et al. are analogous art because they are from the same field of endeavor of DSL transmission.

At the time of the invention it would have been obvious to one of ordinary skill in the art to use Henderson et al.'s reference wire (see figure 4 or 5) technique in Tsatsanis et al. multiline transmission technique (fig 2).

The motivation to combine would have been to have a significant increase in speed for data transmission and the total data rate for transmission over twisted pairs can approach three times the data rate of previous data rate, substantially reducing the time for data transmission. By designating a common wire to support a plurality of lines, then more lines transmit data to provide much desired higher data rates.

As per claim 27, Tsatsanis et al. discloses a method of providing high speed DSL service wherein vectoring transmissions is performed using a first vectoring unit and a second vectoring unit coupled to the opposite ends of the multiple loop segment (see figure 2).

As per claim 28, Tsatsanis et al. discloses a method of providing high speed DSL service, wherein vectoring transmissions across the multiple loop segment comprises one-sided vectoring (see figure 5).

As per claim 29, Tsatsanis et al. discloses a method of providing high speed DSL service, wherein vectoring transmissions across the multiple loop segment comprises one-sided vectoring (see figure 5).

As per claim 30, Tsatsanis et al. discloses a method of providing high speed DSL service, wherein the vectored transmissions across the multiple loop segment utilize an

expanded frequency spectrum on at least one channel (see paragraph 70, and figure 2, block 208).

As per claim 31, Tsatsanis et al. discloses a method of providing high speed DSL service, providing vectoring control signals to the multiple loop segment.

As per claim 35, Tsatsanis et al. discloses a method of providing high speed DSL service, providing impedance matching circuits at each end of the multiple loop segment (see figure 12).

As per claim 36, Tsatsanis et al. discloses a method of providing high speed DSL service, wherein the loops are bonded using one of the following bonding protocols: TDIM bonding; Ethernet bonding; ATM bonding; or the G.bond protocol (see twisted pair, paragraph 49, line 5).

As claim 37 and 38, Tsatsanis et al. discloses a first and second impedance matching circuit includes selected impedance placed between each wire and each other wire (see page 24).

6. Claims 8-9, 18-19, 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsatsanis et al. (US 2006/0056522 A1) in view of Henderson et al. (6678375) further in view of Kerpez (US 7106833 B2).

As per claims 8 and 9 Tsatsanis et al. and Henderson et al. discloses a DSL system but does not expressly disclose the controller being a dynamic spectrum manager comprising vectoring control means comprising a computer system.

Kerpez discloses a controller being a dynamic spectrum manager (see figure 2, block 100 and column 6, lines 21-22) comprising vectoring control means (see column 11, lines 45-47) comprising a computer system (see figure 2, block 100).

Tsatsanis et al., Henderson et al. and Kerpez are analogous art because they are from the same field of endeavor of management of digital subscriber lines.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use Kerpez's dynamic spectrum manager (see figure 2, block 100 and column 6, lines 21-22) in conjunction with Tsatsanis et al.'s transceivers (see figure 11, block 1100) for the management of digital subscriber lines.

The motivation to combine would have been to have a system for provisioning and correcting crosstalk interference in order to optimize the performance of one or more digital subscriber lines in a cable.

As per claim 18, Tsatsanis et al. and Henderson et al. discloses a DSL system but does not expressly disclose the controller being a dynamic spectrum manager.

Kerpez discloses a controller being a dynamic spectrum manager (see figure 2, block 100 and column 6, lines 21-22).

Tsatsanis et al., Henderson et al. and Kerpez are analogous art because they are from the same field of endeavor of management of digital subscriber lines.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use Kerpez's dynamic spectrum manager (see figure 2, block 100 and column 6, lines 21-22) in conjunction with Tsatsanis et al.'s transceivers (see figure 11, block 1100) for the management of digital subscriber lines.

The motivation to combine would have been to have a system for provisioning and correcting crosstalk interference in order to optimize the performance of one or more digital subscriber lines in a cable.

As per claim 19, Tsatsanis et al. and Henderson et al. discloses a DSL system but does not expressly disclose the controller comprises frequency bandwidth control means for regulating the frequency bandwidth used in transmissions across the multiple segment.

Kerpez discloses a controller having frequency bandwidth control means for regulating the frequency bandwidth used in transmissions across the segment (see figure 2, block 100 and column 6, lines 21-22).

Tsatsanis et al., Henderson et al. and Kerpez are analogous art because they are from the same field of endeavor of management of digital subscriber lines.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use Kerpez's frequency bandwidth control means for regulating the frequency bandwidth used in transmissions across the segment (see figure 2, block 100 and column 6, lines 21-22) in conjunction with Tsatsanis et al.'s transceivers (see figure 11, block 1100) for the management of digital subscriber lines.

The motivation to combine would have been to have a system for provisioning and correcting crosstalk interference in order to optimize the performance of one or more digital subscriber lines in a cable.

As per claim 32-34, Tsatsanis et al. and Henderson et al. discloses a method of providing high speed DSL service, but does not expressly disclose the controller being a dynamic spectrum manager and DSM center and controller.

Kerpez discloses a controller being a dynamic spectrum manager and DSM center and controller (see figure 2, block 100 and column 6, lines 21-22).

Tsatsanis et al., Henderson et al. and Kerpez are analogous art because they are from the same field of endeavor of management of digital subscriber lines.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use Kerpez's dynamic spectrum manager and DSM center and controller (see figure 2, block 100 and column 6, lines 21-22) in conjunction with Tsatsanis et al.'s transceivers (see figure 11, block 1100) for the management of digital subscriber lines.

The motivation to combine would have been to have a system for provisioning and correcting crosstalk interference in order to optimize the performance of one or more digital subscriber lines in a cable.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See form 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ABDULLAH RIYAMI whose telephone number is (571)270-3119. The examiner can normally be reached on Monday through Thursday 8am-5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy D. Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Abdullah Riyami/
Examiner, Art Unit 2616

/Huy D. Vu/
Supervisory Patent Examiner, Art Unit 2616